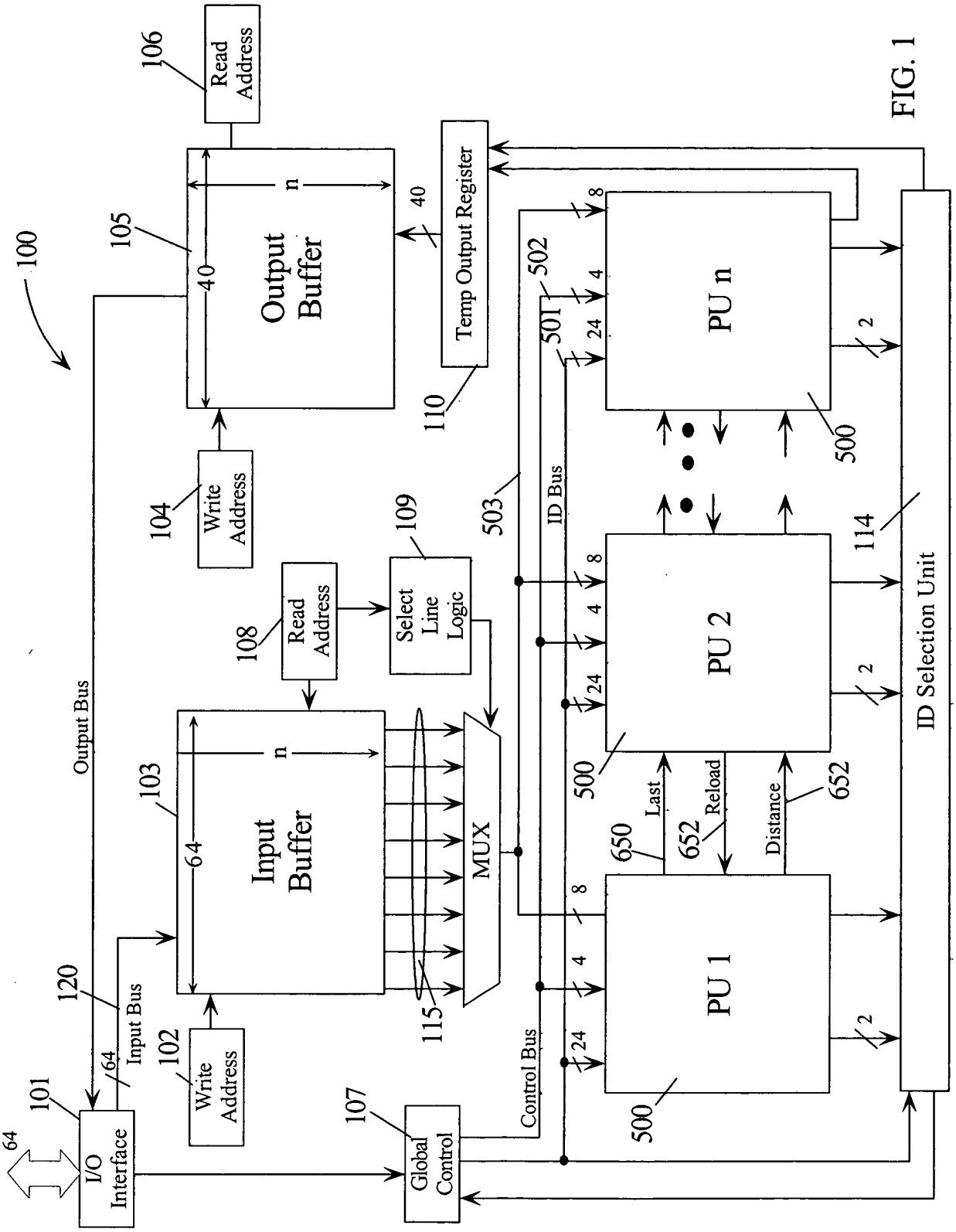
100
101
I/O Interface
64
102
Write Address
103
Input Buffer
n
64
104
Write Address
105
Output Buffer
n
40
106
Read Address
107
Global Control
108
Read Address
109
Select Line Logic
110
Temp Output Register
40
114
ID Selection Unit
115
MUX
120
Input Bus
64
Output Bus
500
PU 1
PU 2
PU n
501
24
502
ID Bus
503
Control Bus
650
652
Last
Reload
Distance
652
8
4
2

FIG. 1

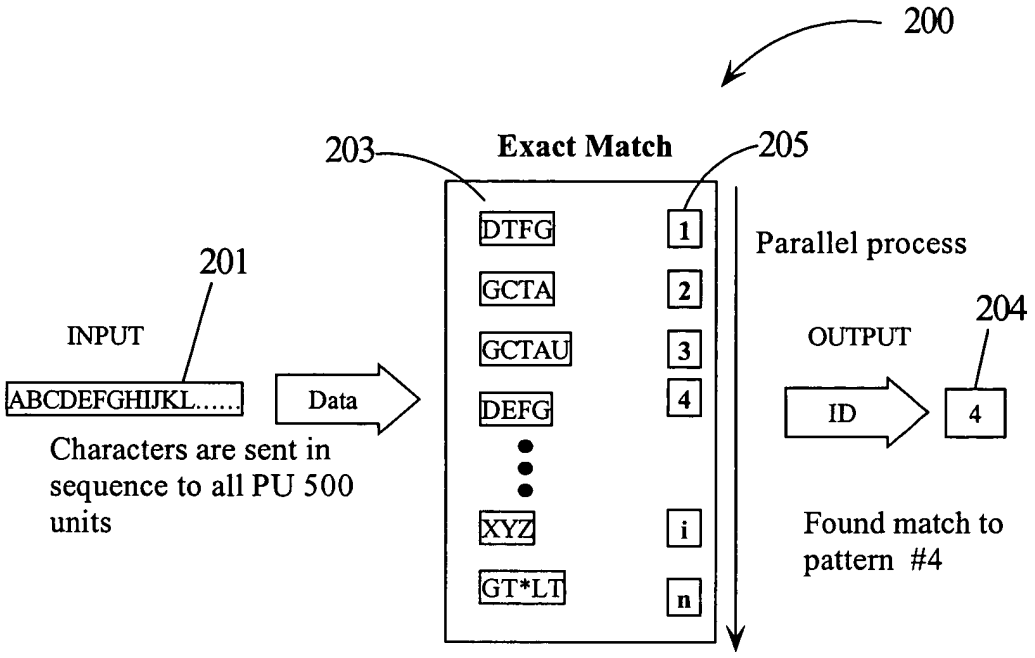
200
203
Exact Match
205
DTFG
GCTA
GCTAU
DEFG
XYZ
GT*LT
1
2
3
4
i
n
Parallel process
201
INPUT
ABCDEFGHIJKL.....
Data
Characters are sent in sequence to all PU 500 units
OUTPUT
204
ID
4
Found match to pattern #4

FIG 2A

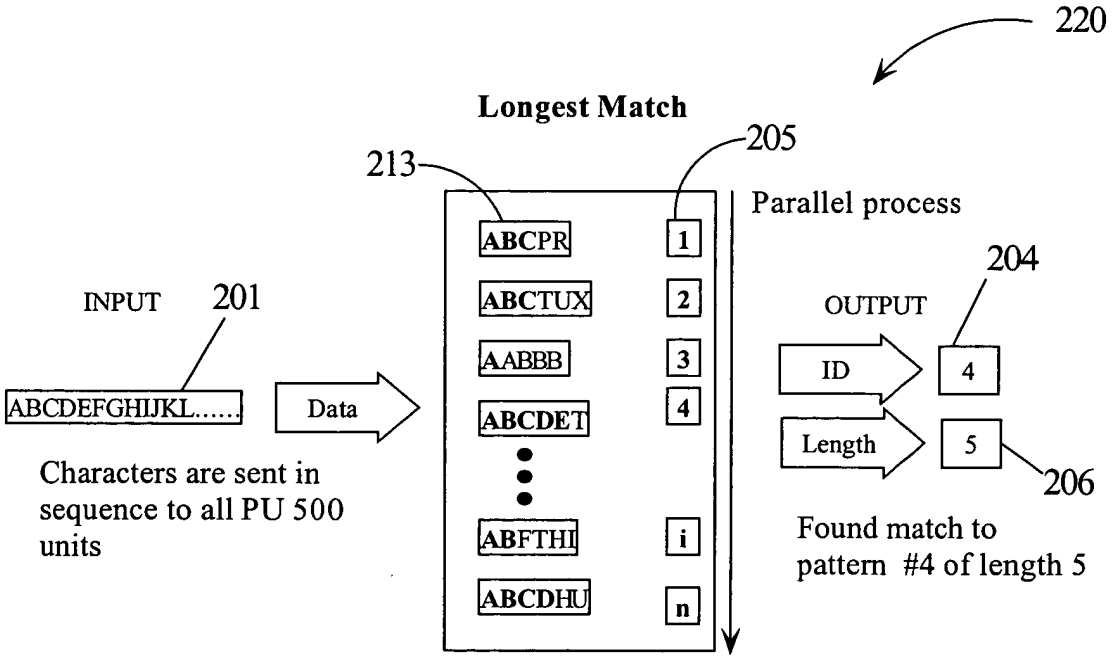
220
Longest Match
213
205
ABCPR
ABCTUX
AABBB
ABCDET
ABFTHI
ABCDHU
1
2
3
4
i
n
Parallel process
INPUT
201
ABCDEFGHIJKL.....
Data
Characters are sent in sequence to all PU 500 units
OUTPUT
204
ID
4
Length
5
206
Found match to pattern #4 of length 5

FIG 2B

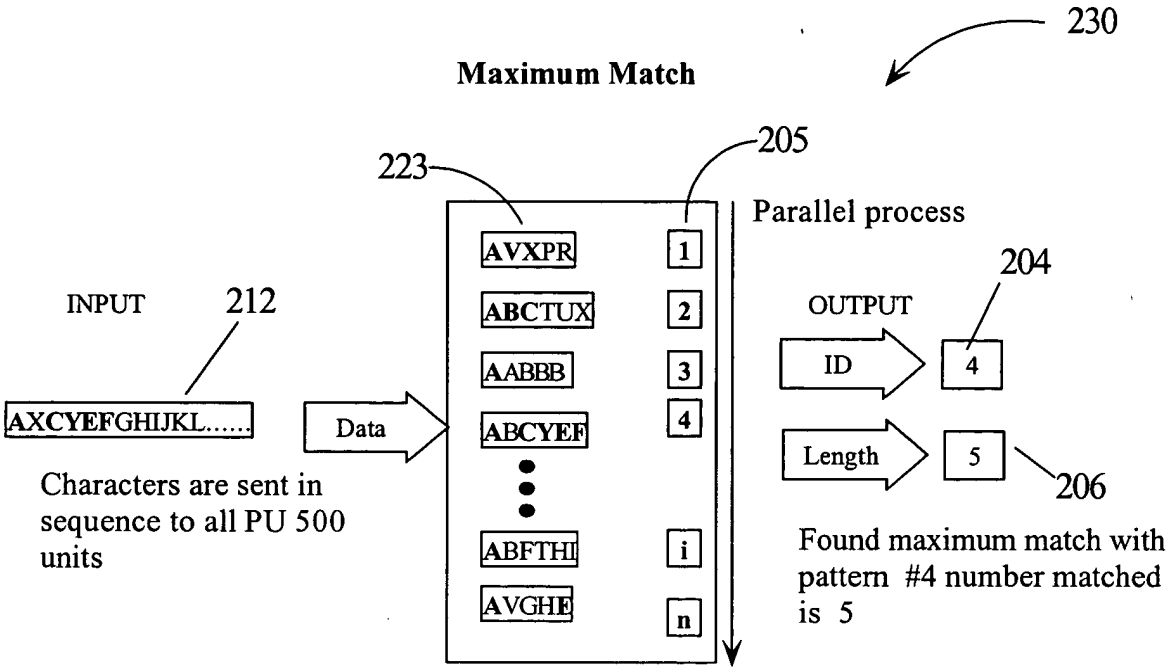
230
Maximum Match
223
205
Parallel process
AVXPR
ABCTUX
AABBB
ABCYEF
ABFTHI
AVGHE
1
2
3
4
i
n
INPUT
212
AXCYEFGHIJKL.....
Data
Characters are sent in sequence to all PU 500 units
OUTPUT
204
ID
4
Length
5
206
Found maximum match with pattern #4 number matched is 5

FIG 2C

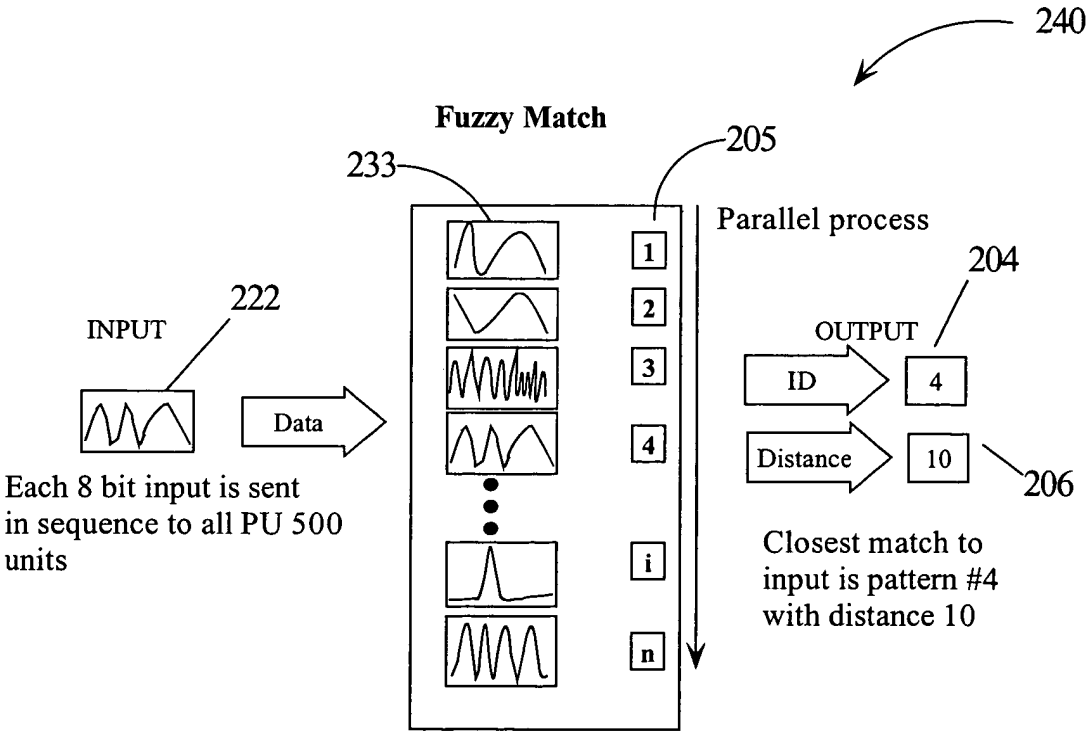
240
Fuzzy Match
233
205
Parallel process
1
2
3
4
i
n
INPUT
222
Data
Each 8 bit input is sent in sequence to all PU 500 units
OUTPUT
204
ID
4
Distance
10
206
Closest match to input is pattern #4 with distance 10

FIG 2D

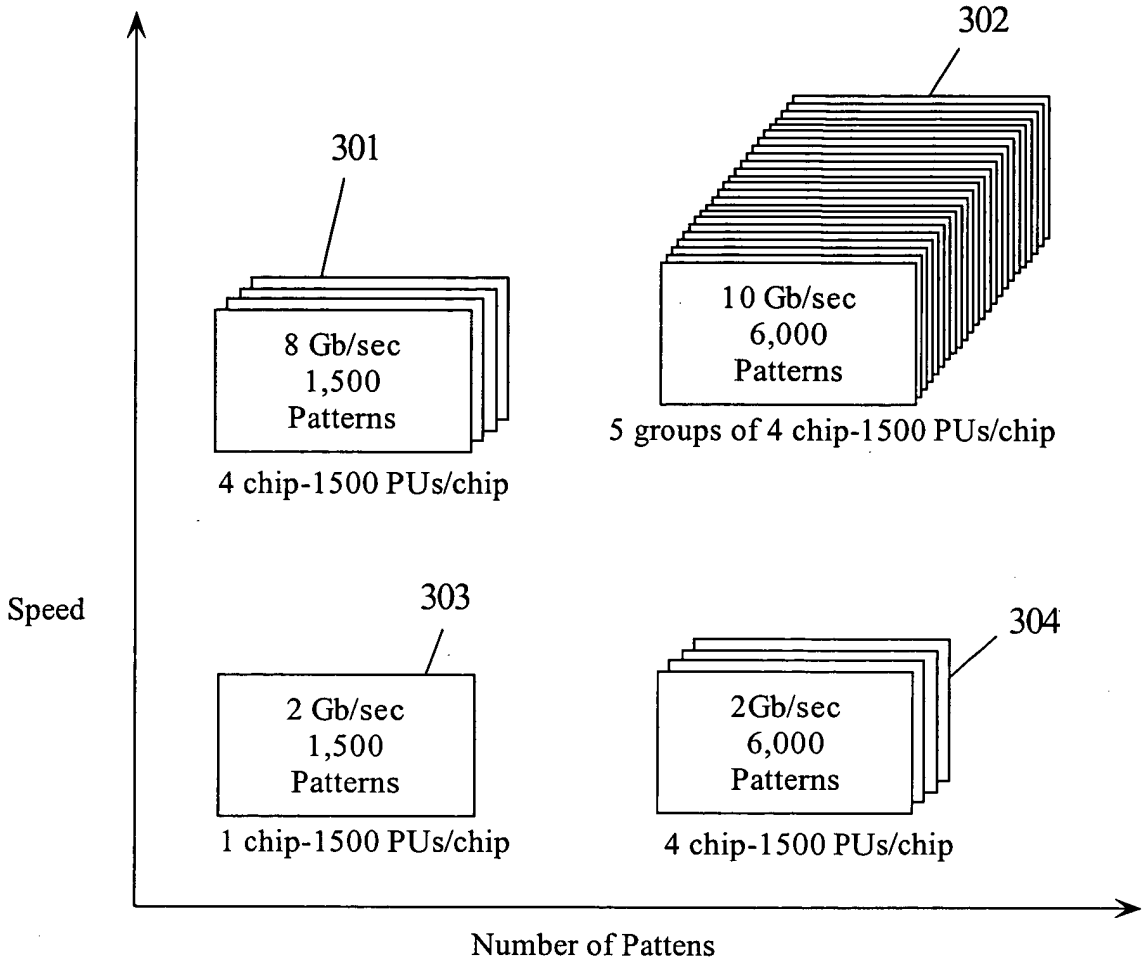
302
301
8 Gb/sec
1,500
Patterns
10 Gb/sec
6,000
Patterns
4 chip-1500 PUs/chip
5 groups of 4 chip-1500 PUs/chip
Speed
303
304
2 Gb/sec
1,500
Patterns
2Gb/sec
6,000
Patterns
1 chip-1500 PUs/chip
4 chip-1500 PUs/chip
Number of Pattens

FIG. 3

PPDE 100 Technical Features

Frequency	0 to 250 MHz
Bandwidth	2Gb/sec at 250 MHz
Compute Power	1.25 TOPS Equivalent
Power Consumption	300mW at 250MHz
Power Supply Vlotage	1.5 V internal (2.5 and 3.3 V compatible)
Technology	CMOS .13 Micron
I/O Pins	88
Die Size	8mm X 8mm
Interface	Fexible interface: max. 64 bits at 66 MHz (max. rate: 4Gb/sec)

FIG. 4

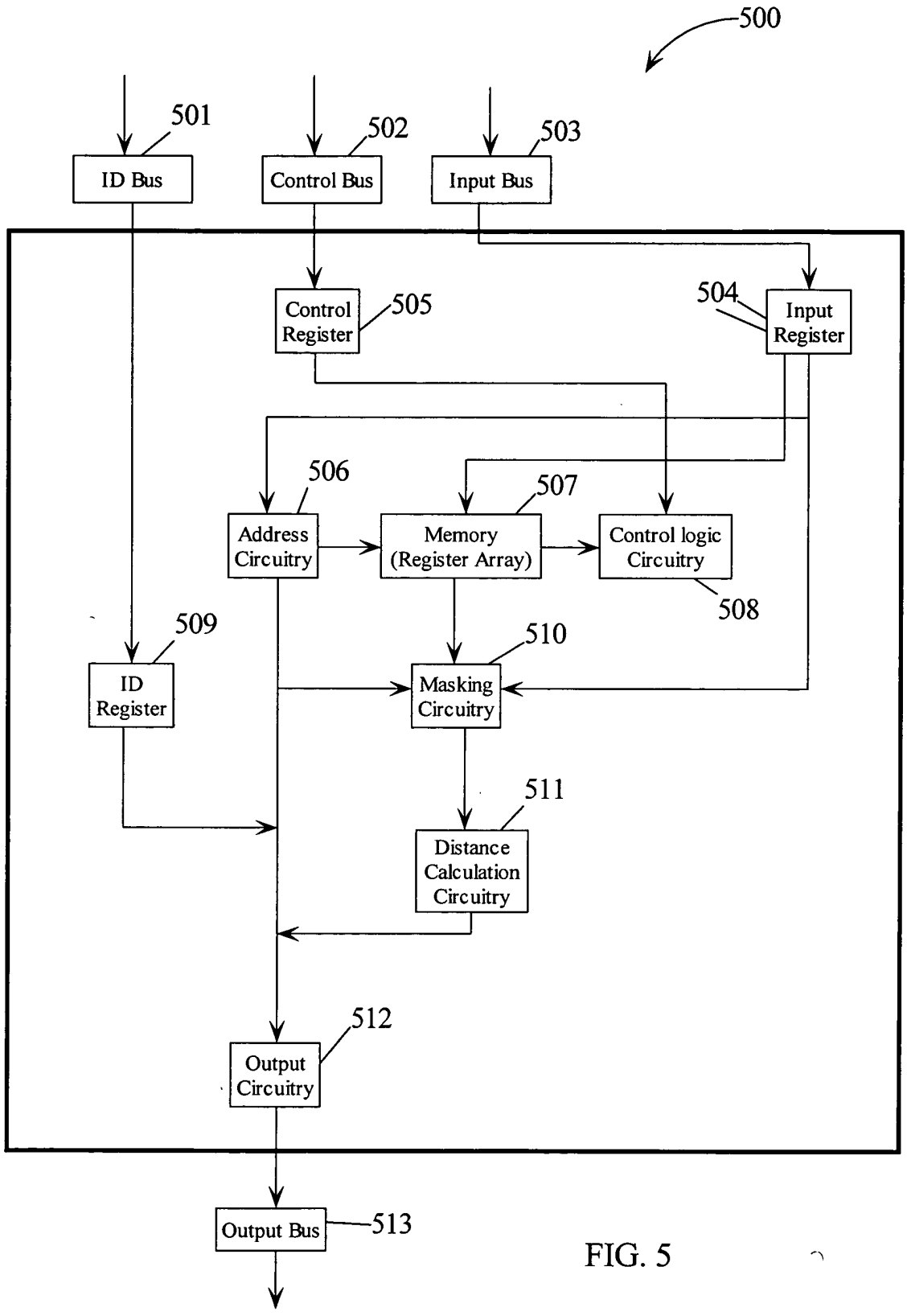
500
501
ID Bus
502
Control Bus
503
Input Bus
Control Register
505
504
Input Register
506
Address Circuitry
507
Memory (Register Array)
Control logic Circuitry
508
509
ID Register
510
Masking Circuitry
511
Distance Calculation Circuitry
512
Output Circuitry
Output Bus
513

FIG. 5

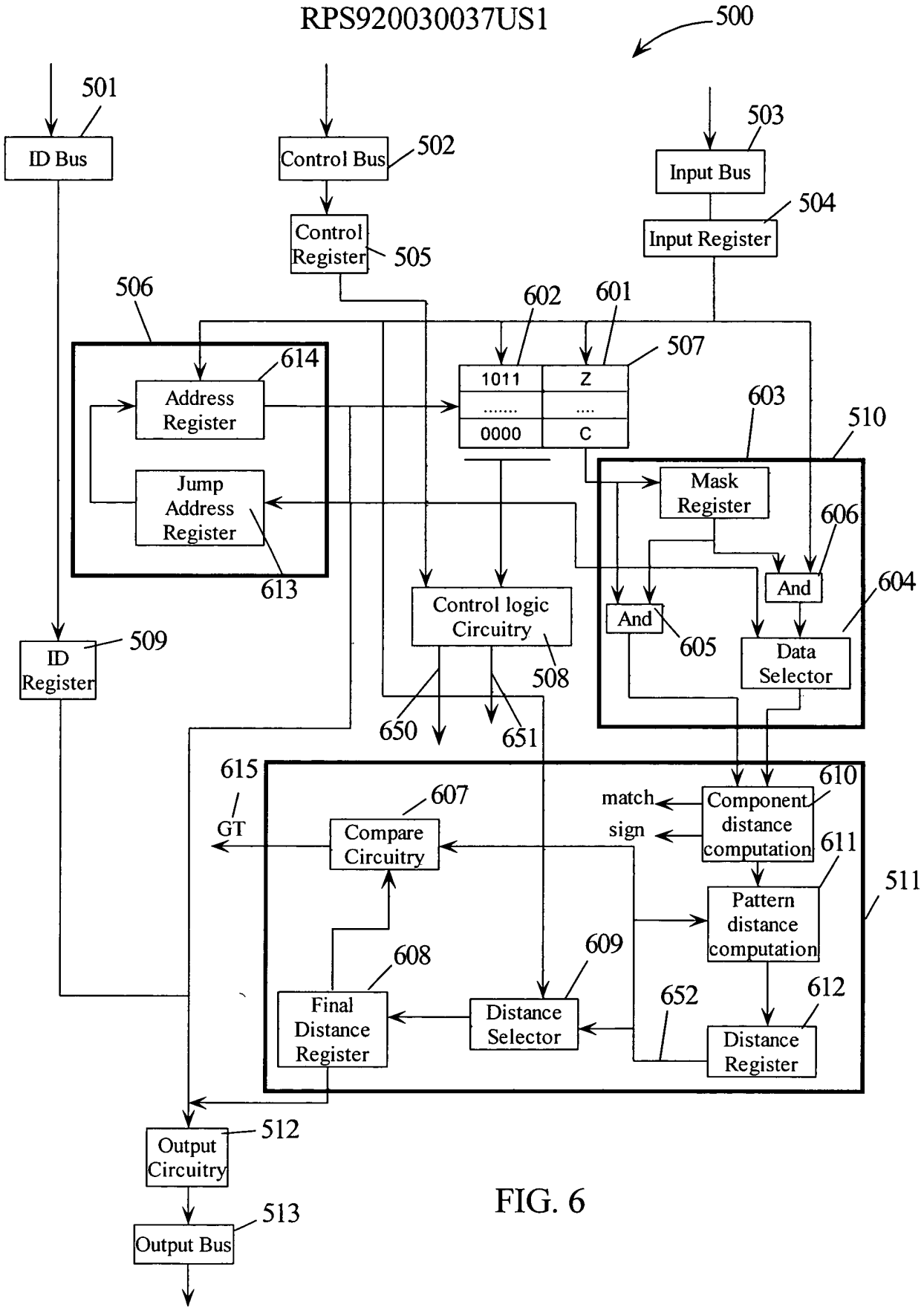
500
501
ID Bus
Control Bus
502
503
Input Bus
504
Input Register
Control Register
505
506
602
601
507
614
Address Register
1011
Z
.....
....
0000
C
603
510
Mask Register
606
Jump Address Register
613
And
604
Control logic Circuitry
And
605
Data Selector
ID Register
509
508
650
651
615
610
607
match
GT
Compare Circuitry
sign
Component distance computation
611
511
Pattern distance computation
608
609
652
612
Final Distance Register
Distance Selector
Distance Register
Output Circuitry
512
513
Output Bus

FIG. 6

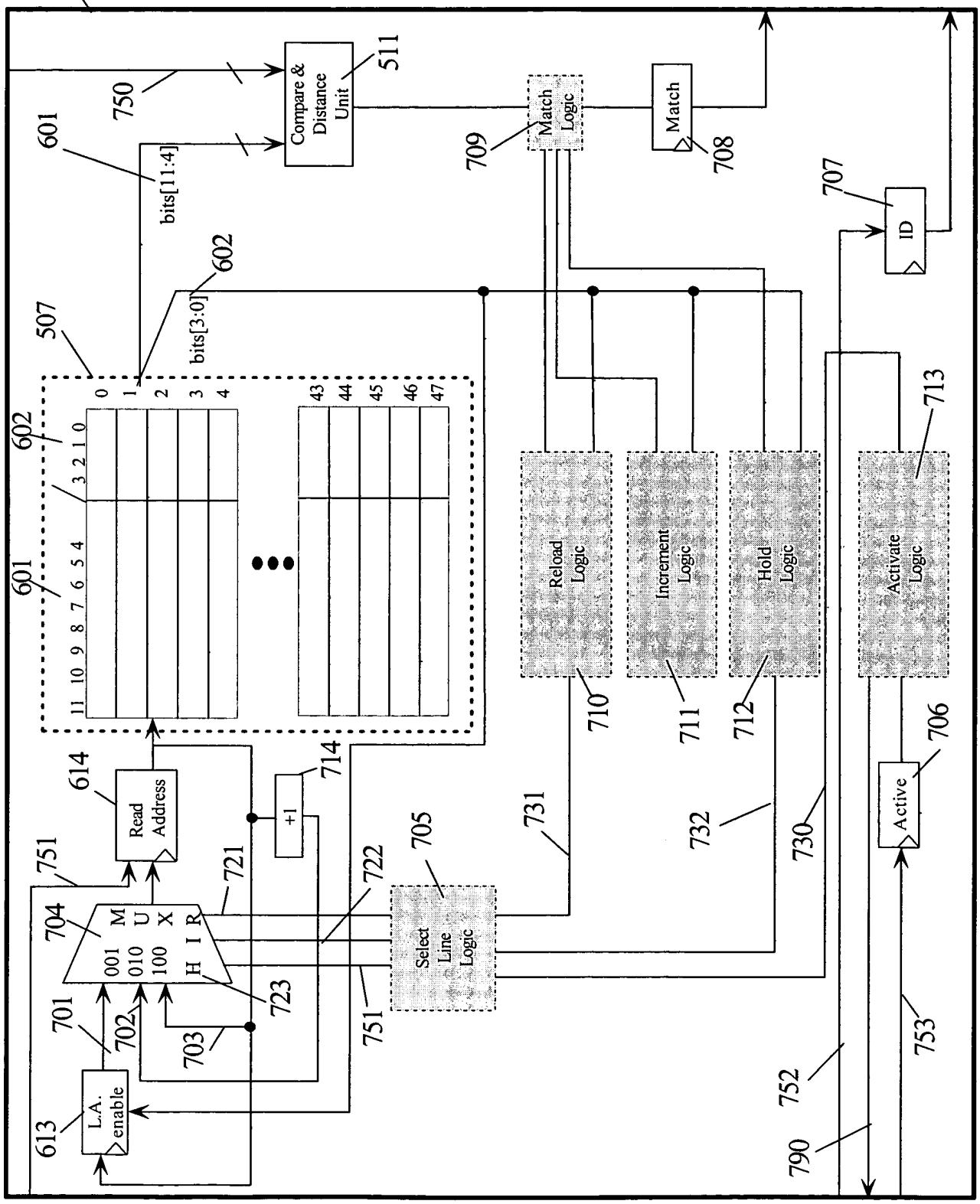
500
Compare & Distance Unit
511
750
601
bits[11:4]
602
bits[3:0]
507
Match Logic
709
Match
708
707
ID
0 1 2 3 4
43 44 45 46 47
11 10 9 8 7 6 5 4
3 2 1 0
Reload Logic
Increment Logic
Hold Logic
Activate Logic
713
710
711
712
706
614
Read Address
714
+1
705
731
732
730
751
721
722
704
M U X
001 010 100
H I R
723
701
702
703
Select Line Logic
Active
753
752
790
613
L.A. enable

FIG. 7

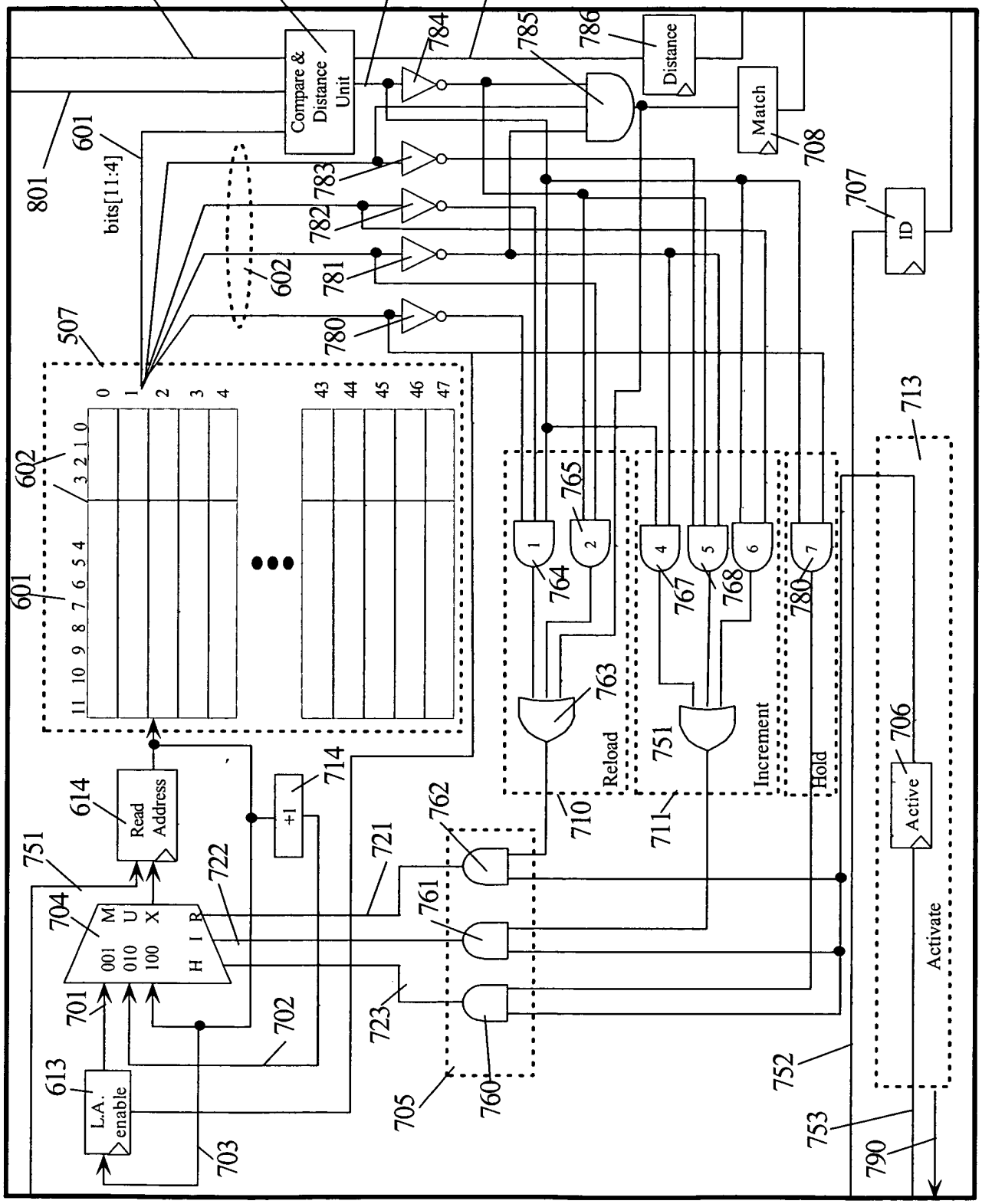
750
511
771
772
784
785
786
Distance
Compare & Distance Unit
Match
708
801
601
bits[11:4]
783
782
781
780
602
507
707
ID
713
Reload
Increment
Hold
710
711
751
763
765
764
767
768
780
706
Active
Activate
614
Read Address
714
+1
762
721
722
761
704
M U X
H I R
001
010
100
701
702
723
705
760
752
753
790
613
L.A. enable
703

FIG. 8

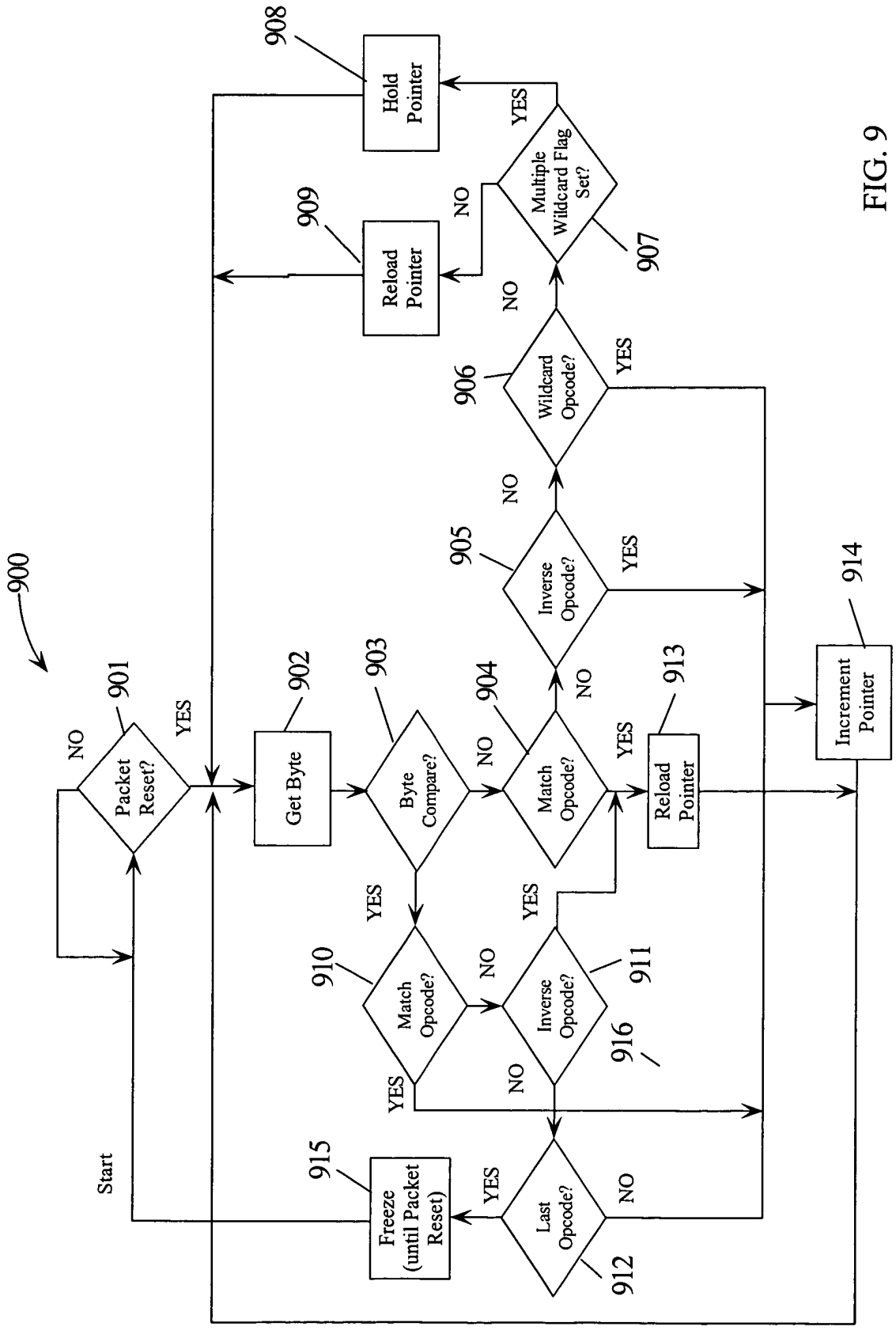
900
Start
Packet Reset?
901
NO
YES
Get Byte
902
Byte Compare?
903
NO
YES
Match Opcode?
904
NO
YES
Inverse Opcode?
905
NO
YES
Wildcard Opcode?
906
NO
YES
Multiple Wildcard Flag Set?
907
NO
YES
Hold Pointer
908
Reload Pointer
909
Match Opcode?
910
NO
YES
Inverse Opcode?
911
NO
YES
Last Opcode?
912
NO
YES
Reload Pointer
913
Increment Pointer
914
Freeze (until Packet Reset)
915
916

FIG. 9

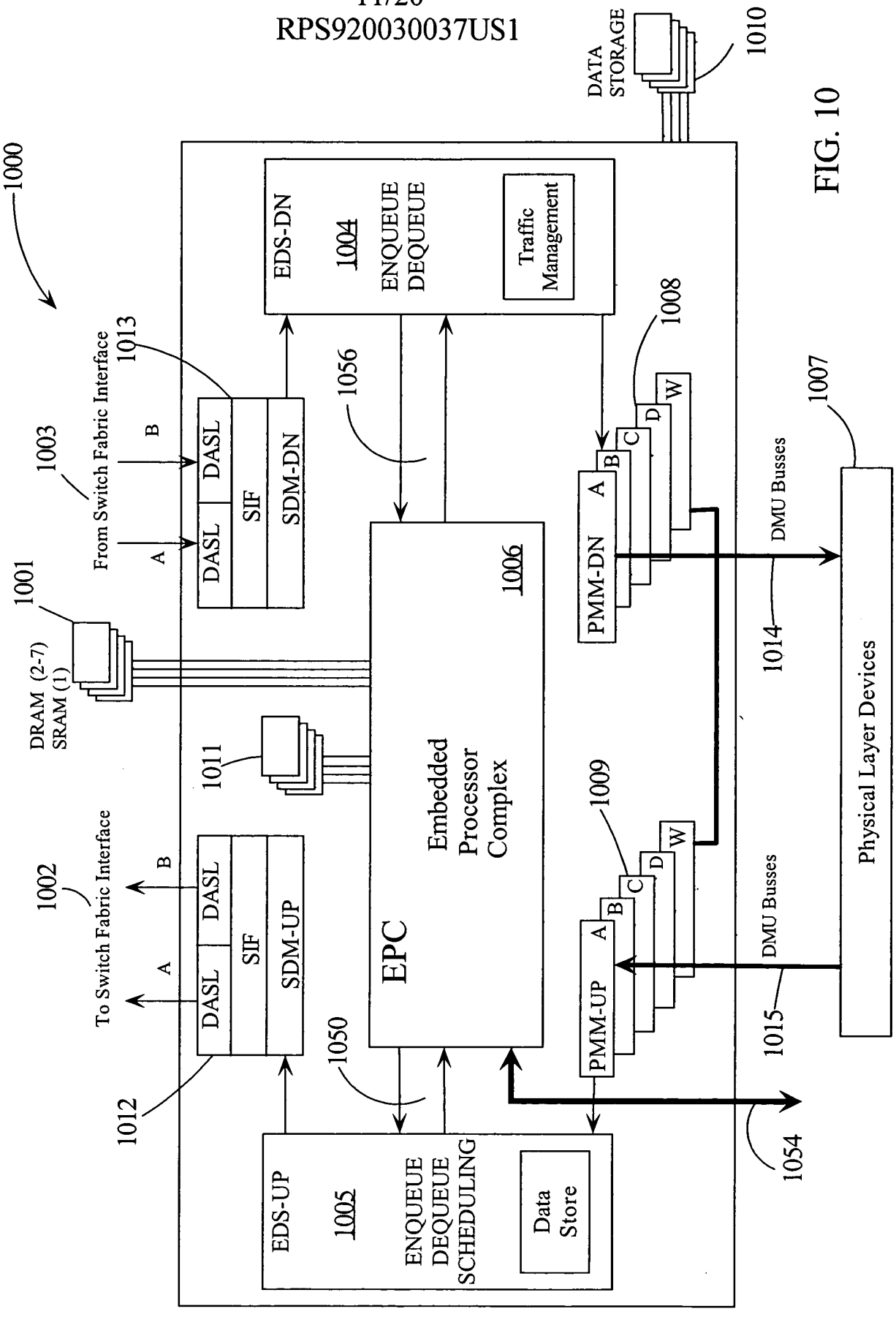
1000
DATA STORAGE
1010
EDS-DN
1004
ENQUEUE
DEQUEUE
Traffic Management
1013
1003
From Switch Fabric Interface
B
A
DASL
DASL
SIF
SDM-DN
1056
1008
PMM-DN
A
B
C
D
W
1001
DRAM (2-7)
SRAM (1)
1006
Embedded
Processor
Complex
DMU Busses
1007
1014
1011
1009
1002
To Switch Fabric Interface
B
A
DASL
DASL
SIF
SDM-UP
EPC
1050
PMM-UP
A
B
C
D
W
DMU Busses
Physical Layer Devices
1012
EDS-UP
1005
ENQUEUE
DEQUEUE
SCHEDULING
Data
Store
1015
1054

FIG. 10

Case 1: Reload if there is NOT a pattern match and the match OPcode is set
Partial expression to match: "ABC"

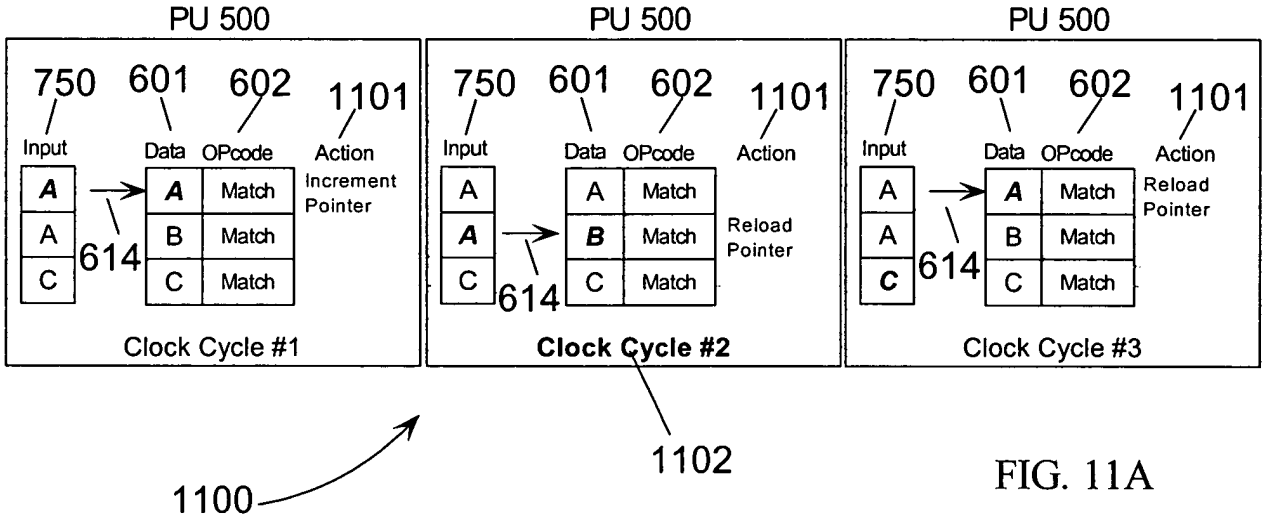

FIG. 11A

Case 2: Reload if there is a pattern match and the inverse OPcode is set for a pattern byte
Partial Expression to match : "C!DE"

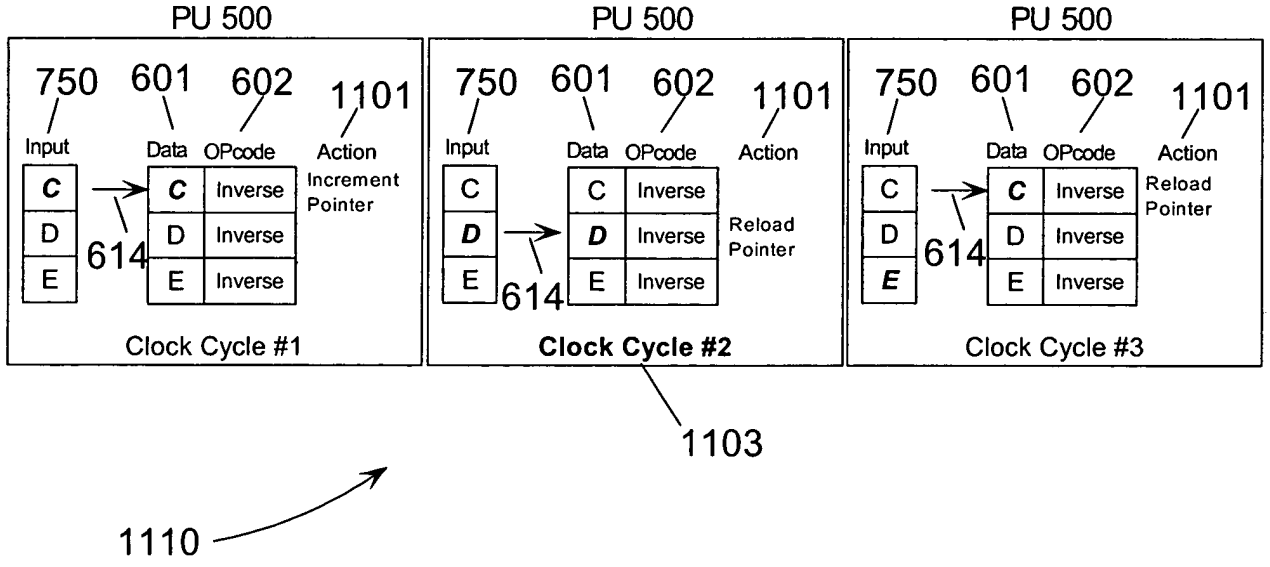

FIG. 11B

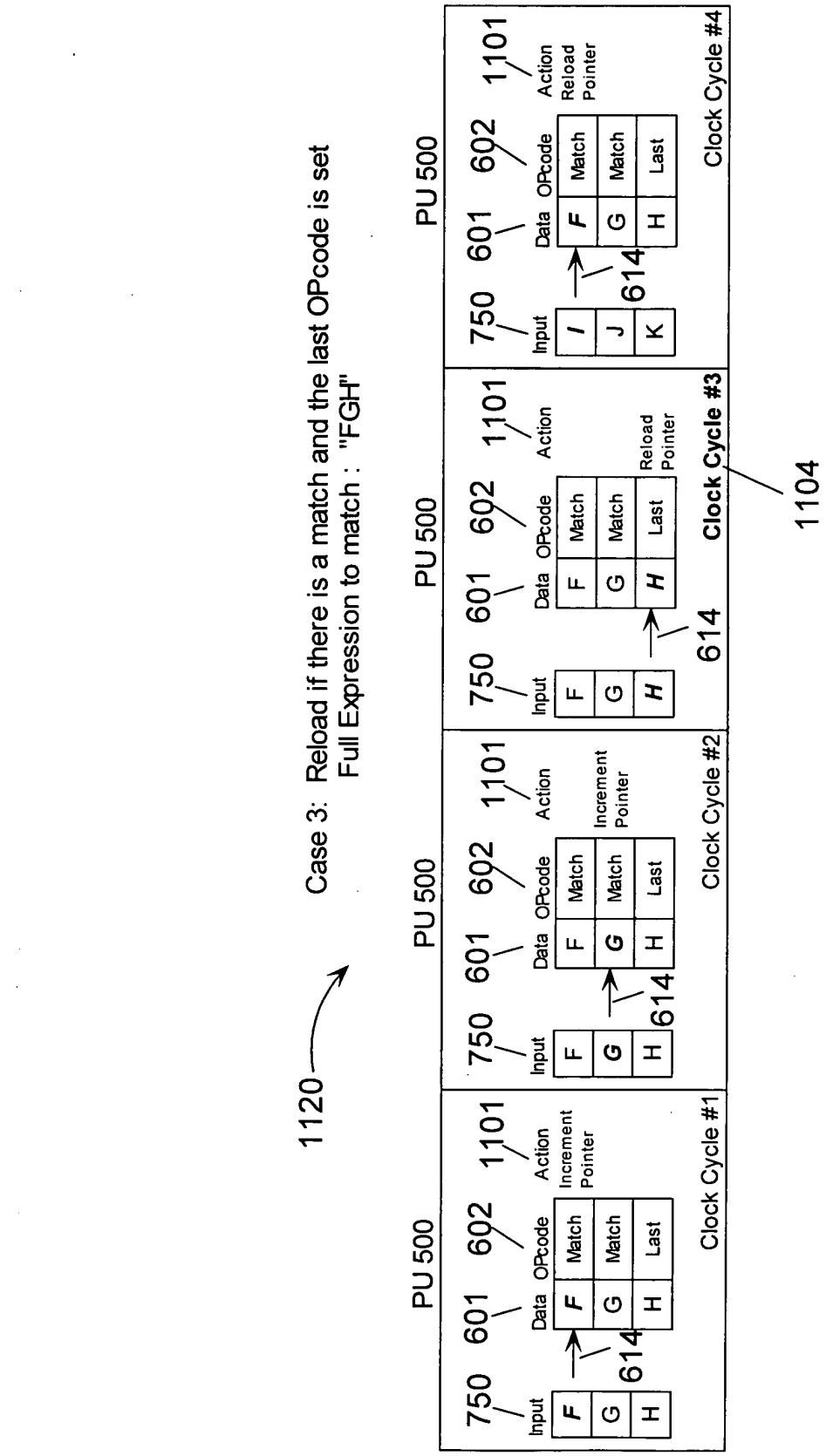
Case 3: Reload if there is a match and the last OPcode is set
Full Expression to match : "FGH"
1120
1104
PU 500
Clock Cycle #1
Clock Cycle #2
Clock Cycle #3
Clock Cycle #4
Input
Data
OPcode
Action
Increment Pointer
Reload Pointer
Match
Last
750
601
602
1101
614
F
G
H
I
J
K

FIG. 11C

Case 4: Increment if there is NOT a pattern match and the inverse OPcode is set
Partial expression to match: "I!LK"

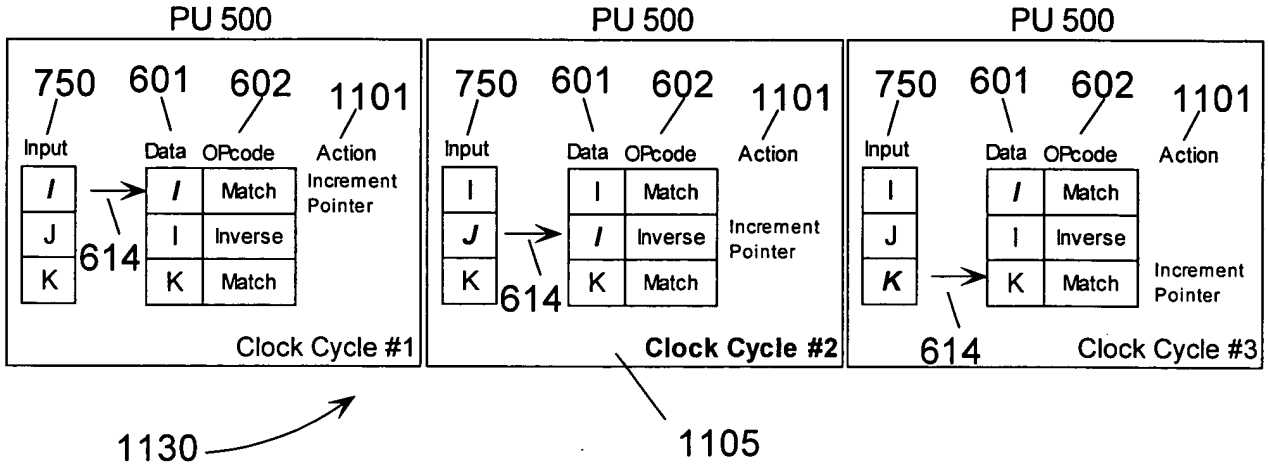

FIG. 11D

Case 5: Increment if there is a pattern match and the match OPcode is set
Partial Expression to match : "LMN"

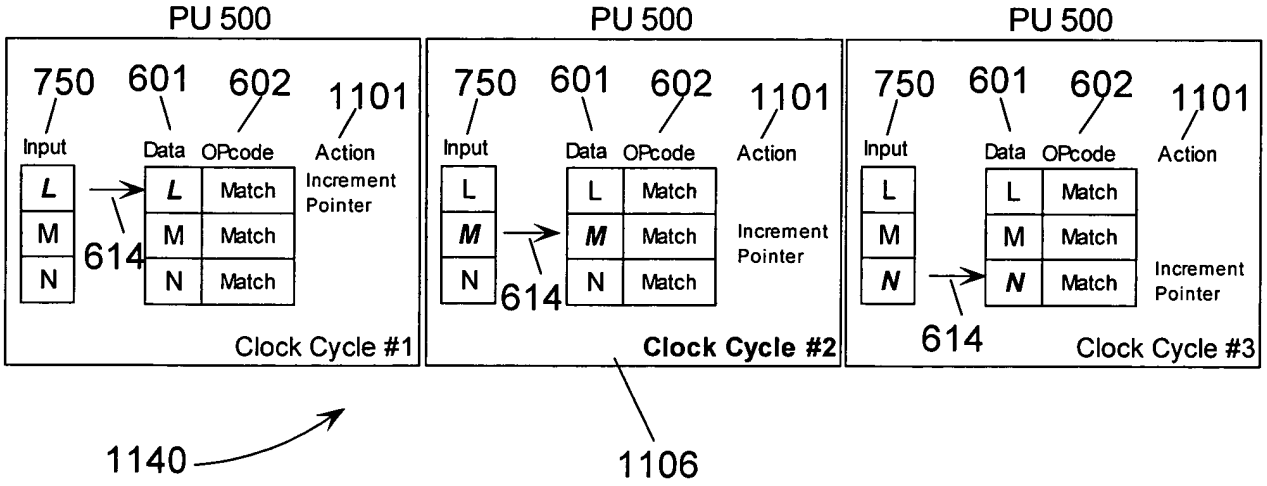

FIG. 11E

Case 6: Increment if there is NOT a pattern match and the wildcard OPcode is set
Partial expression to match: "O•Q"

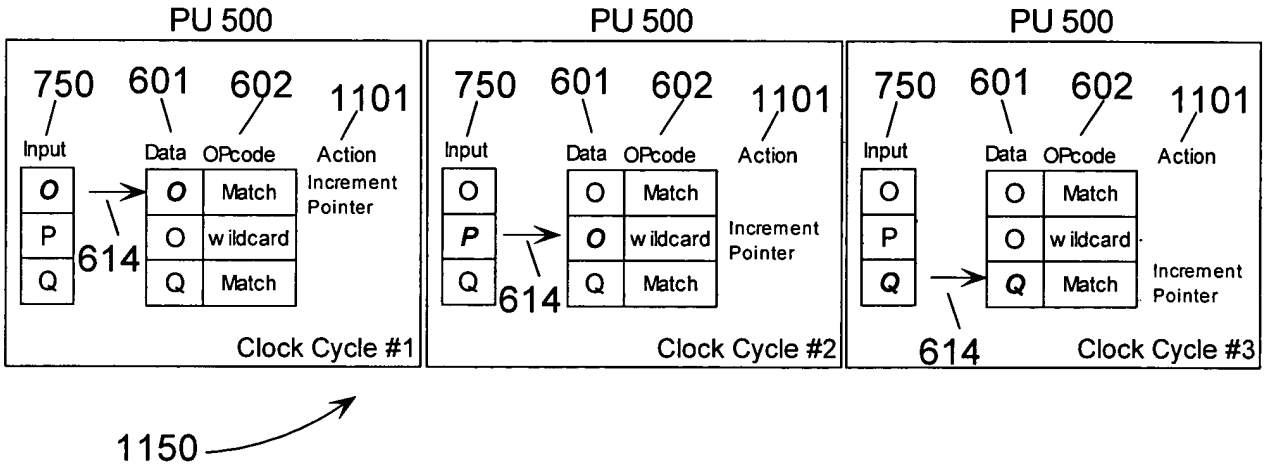

FIG. 11F

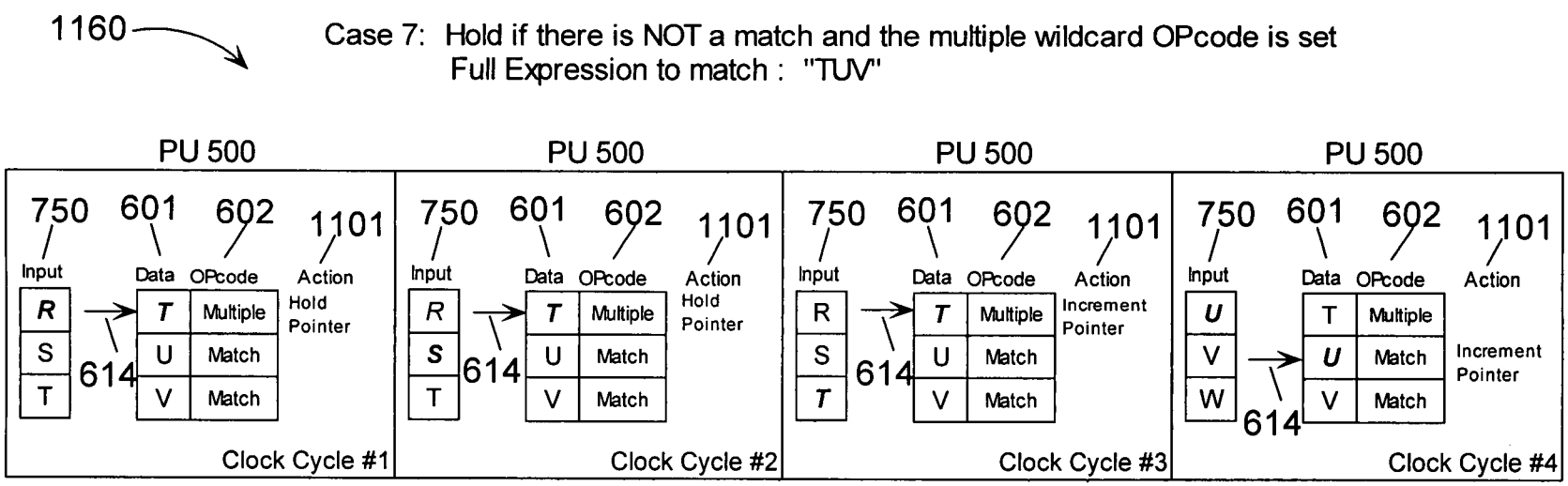
1160
Case 7: Hold if there is NOT a match and the multiple wildcard OPcode is set
Full Expression to match : "TUV"
PU 500
750
601
602
1101
Input
Data
OPcode
Action
R
S
T
614
T
U
V
Multiple
Match
Match
Hold Pointer
Clock Cycle #1
Clock Cycle #2
Increment Pointer
Clock Cycle #3
U
V
W
Clock Cycle #4

FIG. 11G

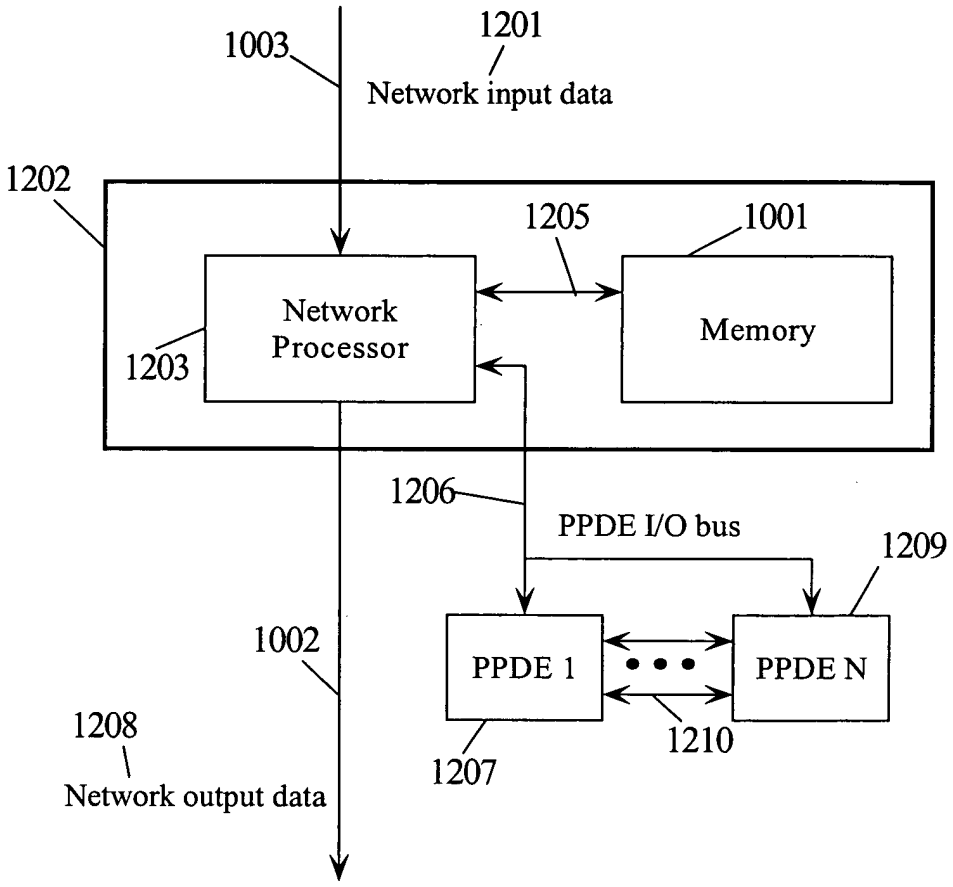
1003
1201
Network input data
1202
1205
1001
Network Processor
Memory
1203
1206
PPDE I/O bus
1209
1002
PPDE 1
PPDE N
1208
1210
1207
Network output data

FIG. 12

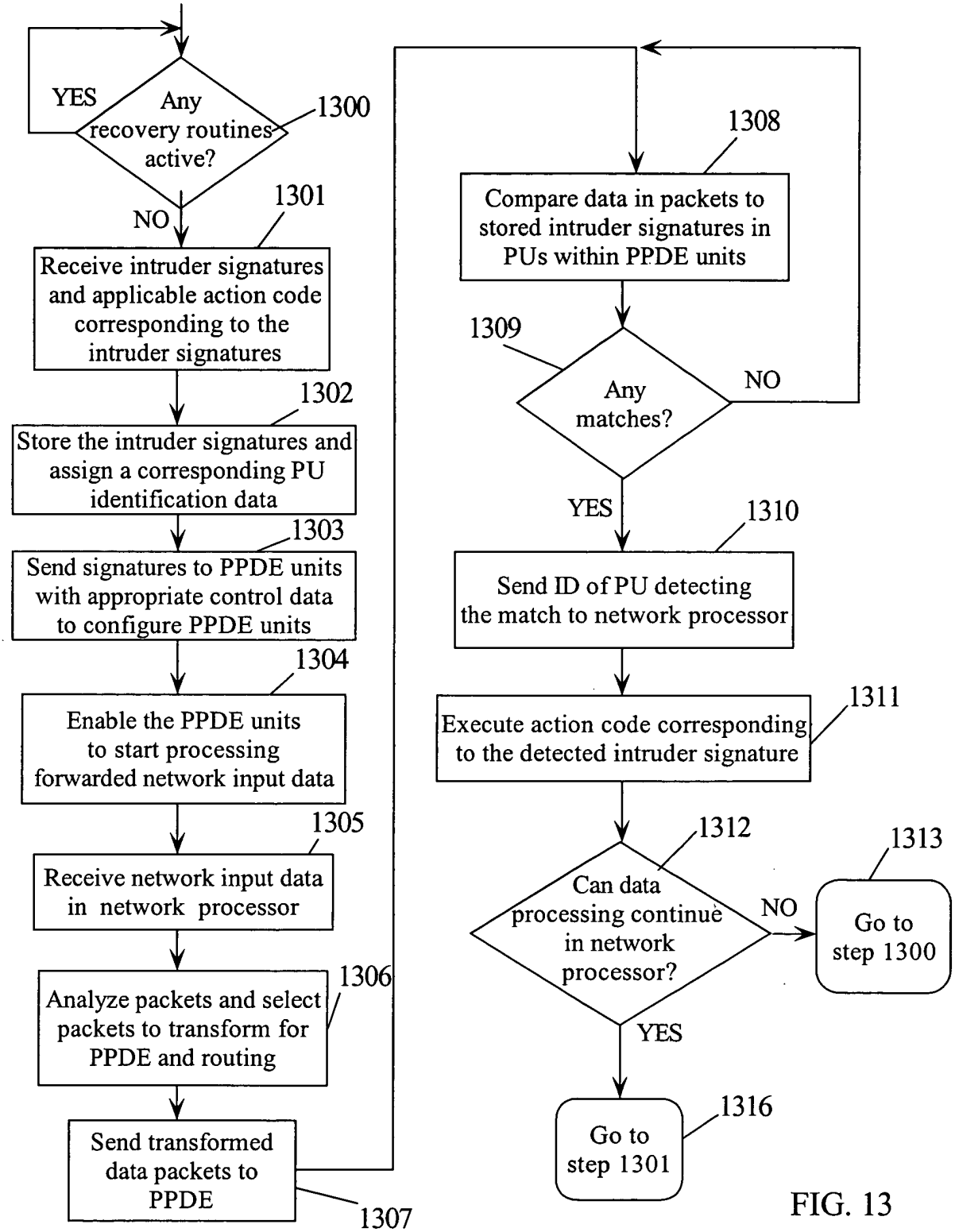
Any recovery routines active?
YES
NO
1300
1301
Receive intruder signatures and applicable action code corresponding to the intruder signatures
1302
Store the intruder signatures and assign a corresponding PU identification data
1303
Send signatures to PPDE units with appropriate control data to configure PPDE units
1304
Enable the PPDE units to start processing forwarded network input data
1305
Receive network input data in network processor
1306
Analyze packets and select packets to transform for PPDE and routing
Send transformed data packets to PPDE
1307
1308
Compare data in packets to stored intruder signatures in PUs within PPDE units
1309
Any matches?
NO
YES
1310
Send ID of PU detecting the match to network processor
1311
Execute action code corresponding to the detected intruder signature
1312
Can data processing continue in network processor?
NO
1313
Go to step 1300
YES
1316
Go to step 1301

FIG. 13

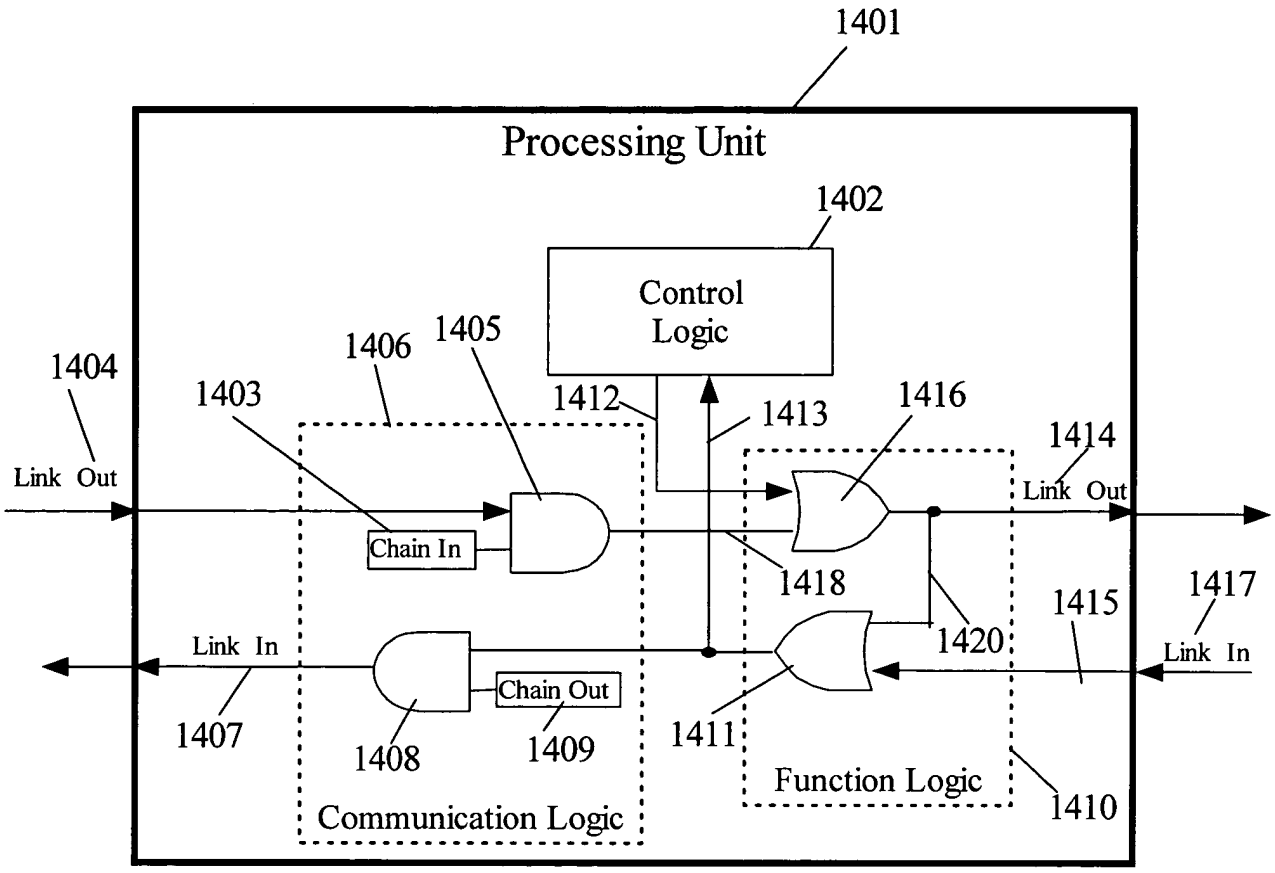
1401
Processing Unit
1402
Control Logic
1404
1403
1406
1405
1412
1413
1416
1414
Link Out
Chain In
1418
Link Out
1417
1415
Link In
1420
Link In
Chain Out
1407
1408
1409
1411
Function Logic
1410
Communication Logic

FIG. 14

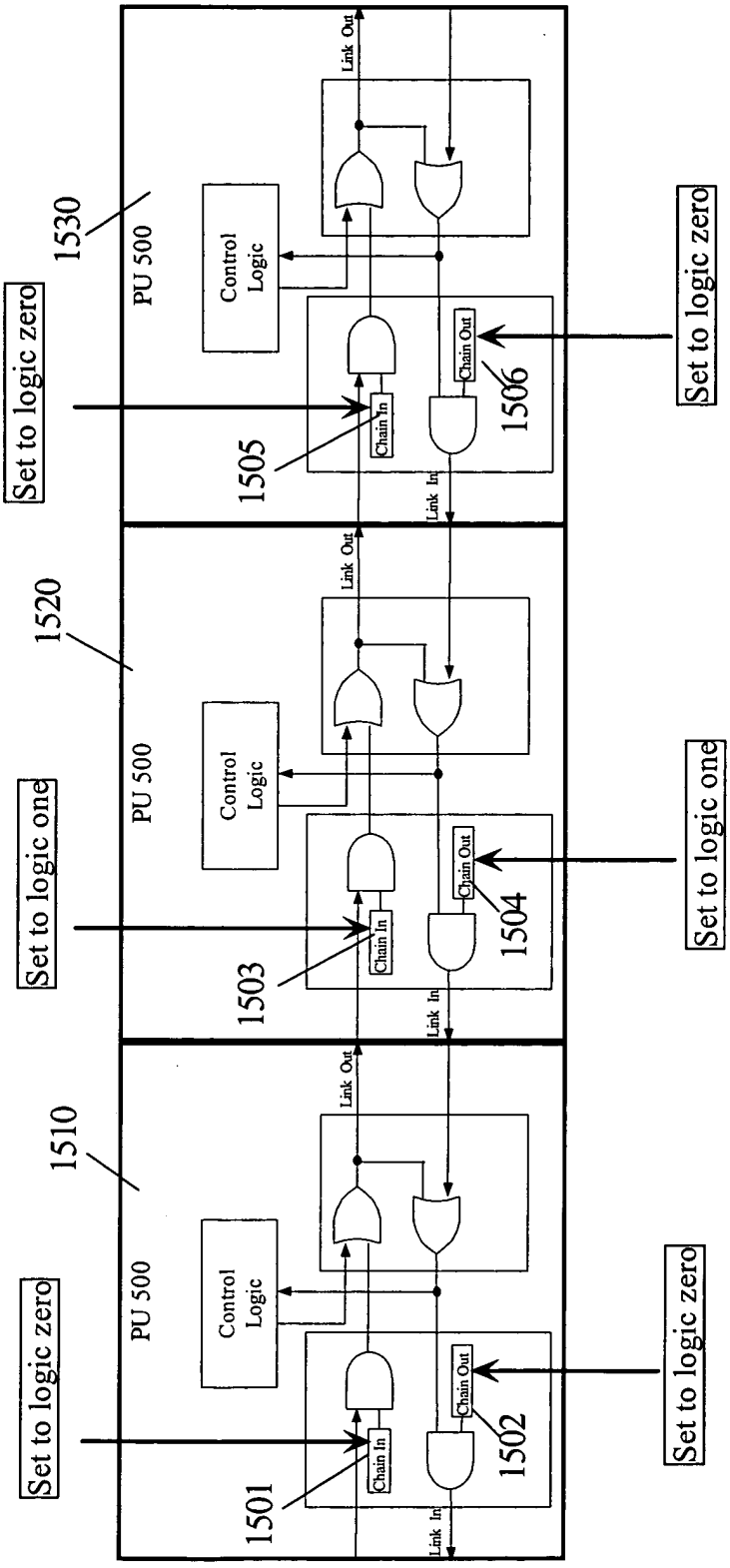
1530
PU 500
Control Logic
Link Out
Link In
Chain In
Chain Out
Set to logic zero
1505
1506
Set to logic zero
1520
PU 500
Control Logic
Link Out
Link In
Chain In
Chain Out
Set to logic one
1503
1504
Set to logic one
1510
PU 500
Control Logic
Link Out
Link In
Chain In
Chain Out
Set to logic zero
1501
1502
Set to logic zero

FIG. 15